REMARKS/ARGUMENTS

The applicant's attorneys appreciate the Examiner's thorough search and remarks.

Responsive to the objection against claim 9, claim 9 has been amended, although it is respectfully submitted that amendment was not necessary because only reverse voltage is blocked, not forward voltage. Withdrawal of the objection is requested.

Responsive to the rejection of claims 9-13 under 35 U.S.C. §112, first paragraph, claim 9 has been amended. Reconsideration is requested.

The Office Action states that "the alleged teaching away is not found in Floyd '716".

Floyd '716 (U.S. 6,090,716) states the following:

> Reference is made to U.S. application Ser. No. 08/415,099, invented by Floyd et al., assigned to Siliconix incorporated, filed Mar. 31, 1995, now U.S. Pat. No. 5,592,005, for a description of the operation of such transistors.
>
> It is the present intent to provide an efficient method for fabricating such transistors of the type described in that patent. Col. 1, lines 43-49.

Thus, Floyd '716 clearly states that the operation of its device is disclosed in U.S. 5,592,005, Floyd '005. The prior response is referring to Floyd '005 which, according to Floyd '716, describes the operation of the device of Floyd '716. The Examiner is invited to revisit the prior response in view of the disclosure of Floyd '005.

In the Office Action, the Examiner has stated that Floyd '716 teaches an N-type gate 58A and a P-type channel.

Floyd '716, however, states the following:

> The polysilicon layer 58 is etched back to a thickness of approximately 5000Å as measured from the oxide 56 overlying the mesas 48. Next, the polysilicon layer 58 is implanted with phosphorous at a dosage of 1.0 E15 at 80 KeV, and a drive in step is undertaken to drive the phosphorous into the polysilicon layer 58. Next, a boron nitride deposition is undertaken with a soak to drive boron into the polysilicon layer 58. The 500Å thickness of the oxide layer 56 provides that boron doping will properly reach the polysilicon in the bottom of each trench 46 without going across the oxide. Col. 2, lines 55-65; see also Fig. 6.

Boron is a known P-type dopant. Floyd '716 does not explain the purpose of the phosphorous implant, but careful reading of Floyd '716 makes it clear that the gate electrodes are intended to be P-type in that Floyd '716 emphasizes that oxide layer is thick enough to allow "boron doping" to reach "the polysilicon in the bottom of each trench 46".

Note further that Floyd '716 calls for phosphorous doping to be carried out at 80KeV, col. 2, lines 58-59, while trenches 46 are about 3μm deep, col. 2, lines 38-41. Given the low energy level called for by Floyd '716, it is suggested that Floyd '716 does not intend to dope gate electrode 58A N-type because gate electrodes 58A lie deep inside trenches 46.

Reconsideration of the rejections based on arguments set forth in the last response as well as arguments set forth herein is requested.

The application is believed to be in condition for allowance. Such action is earnestly solicited.

EXPRESS MAIL CERTIFICATE

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail to Addressee (mail label # EV889348808US) in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on October 26, 2007

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Respectfully submitted,

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